

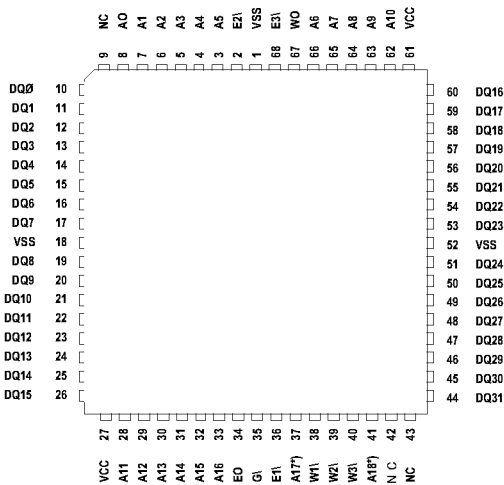
**Features**

- 512Kx32 bit CMOS Static Random Access Memory
- Fast Access Times: 20, 25, 35, 45, and 55ns
- Individual Byte Selects (x8, x16, x32)
- Data Retention Function, ED18C32512LP
- Output Enable Function
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks
- High Density MCM-C Packaging <0.99 in. sq.
  - 68 lead JLCC, No. 351
  - 68 lead CQFP, No. 405
  - Multiple Ground Pins for Maximum Noise Immunity
- Single +5V (±10%) Supply Operation
- DSCC Drawing 5962-94611

**512Kx32 High Speed Static RAM**

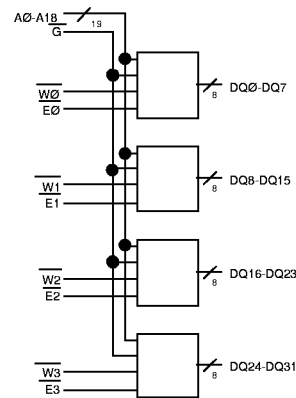
The ED18C32512CA, a high speed, high performance, four megabit density Static RAM organized as 512Kx32 bits, contains four 512Kx8 SRAMs mounted in a package. Four Chip Enables are provided to independently enable each of the four bytes. Reading or writing can be executed on an individual byte or any combination of bytes through proper use of the chip and write enables. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use. The ED18C32512CA is offered in a 68 lead JLCC package which enables 4 megabits of memory to be placed in less than 0.99 square inches of space, respectively. The device may be screened in accordance with MIL-PRF-38535. The ED18C32512CA is pin for pin compatible with the ED18C32128C, providing an upgrade path.

**Pin Configurations and Block Diagram**



**Pin Names**

- A0-A18 Address Inputs
- E0-E3 Chip Enables
- W0-W3 Write Enables
- G Output Enable
- DQ0-DQ31 Common Data Input/Output
- VCC Power (+5V±10%)
- VSS Ground
- NC No Connection



**Electronic Designs Incorporated**

• One Research Drive • Westborough, MA 01581 USA • 508-366-5151 • FAX 508-836-4850 •  
**Electronic Designs Europe Ltd.** • Shelley House, The Avenue • Lightwater, Surrey GU18 5RF  
 United Kingdom • 01276 472637 • FAX: 01276 473748  
<http://www.electronic-designs.com>

### Absolute Maximum Ratings\*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0 °C to +70 °C
Industrial	-40 °C to +85 °C
Military	-55 °C to +125 °C
Storage Temperature	-65 °C to +150 °C
Power Dissipation	4.5 Watts
Output Current	40 mA
Junction Temperature, TJ	175 °C

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

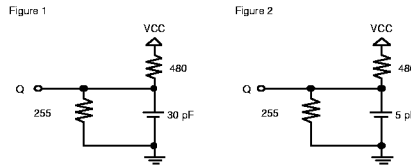
### Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	VCC+0.5	V
Input Low Voltage	VIL	-0.3	--	0.8	V

### AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)



### DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ	Max	Units
Operating Power	ICC1	$\bar{W} = VIL, II/O = 0mA$	20ns	625	800	mA
Supply Current – x32		(4) $\bar{E} = VIL$	25-55ns	450	600	mA
Operating Power	ICC1	$\bar{W} = VIL, II/O = 0mA$	20ns	330	430	mA
Supply Current – x16		(2) $\bar{E} = VIL, (2) \bar{E} \geq VCC - 0.2V$	25-55ns	240	340	mA
Operating Power	ICC1	$\bar{W} = VIL, II/O = 0mA$	20ns	180	280	mA
Supply Current – x8		(1) $\bar{E} = VIL, (3) \bar{E} \geq VCC - 0.2V$	25-55ns	140	240	mA
Standby (TTL) Power	ICC2	(All) $\bar{E} \geq VIH, VIL \geq VIN \geq VIH$		60	125	mA
Supply Current						
Full Standby Power	ICC3	(All) $\bar{E} \geq VCC - 0.2V$	C	50	60	mA
Supply Current		$VIN \geq VCC - 0.2V$ or $VIN \leq 0.2V$	LP	40	45	mA
Input Leakage Current	ILI	$VIN = 0V$ to VCC	--	--	±10	µA
Output Leakage Current	ILO	$V I/O = 0V$ to VCC	--	--	±10	µA
Output High Voltage	VOH	$IOH = -4.0mA$	2.4			V
Output Low Voltage	VOL	$IOL = 8.0mA$			0.45	V

\*Typical: TA=25 °C, VCC=5.0V

### Truth Table

G	E	W	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

### Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	50	pF
Data Lines	CD/Q	20	pF
Chip & Write Enable Lines E, W		20	pF
Output Enable Line	G	50	pF

These parameters are sampled, not 100% tested.

## ED18C32512CA

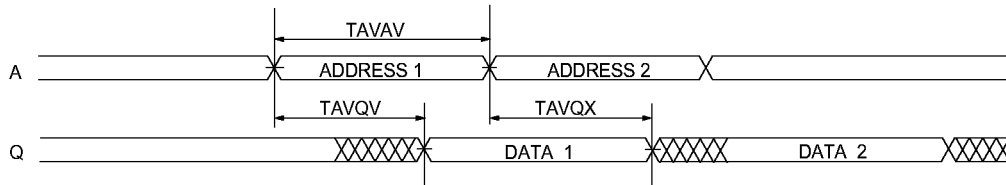
512Kx32 Static Ram

**AC Characteristics Read Cycle**

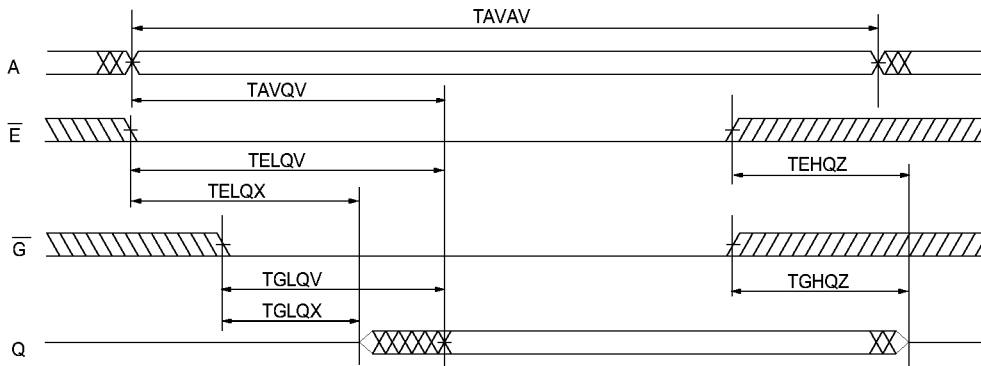
Parameter	Symbol		20ns		25ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	20		25		35		45		55		ns
Address Access Time	TAVQV	TAA		20		25		35		45		55	ns
Chip Enable Access Time	TELQV	TACS		20		25		35		45		55	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		10		12		20		25		25	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		8		10		20		25		25	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		8		10		20		25		25	ns
Chip Enable to Power Up	TELCCH	TPU	0		0		0		0		0		ns
Chip Enable to Power Down	TEHICCL	TPD		20		25		35		45		55	ns

Note 1: Parameter guaranteed, but not tested.

**Read Cycle 1 -  $\overline{W}$  High,  $\overline{G}$ ,  $\overline{E}$  Low**



**Read Cycle 2 -  $\overline{W}$  High**

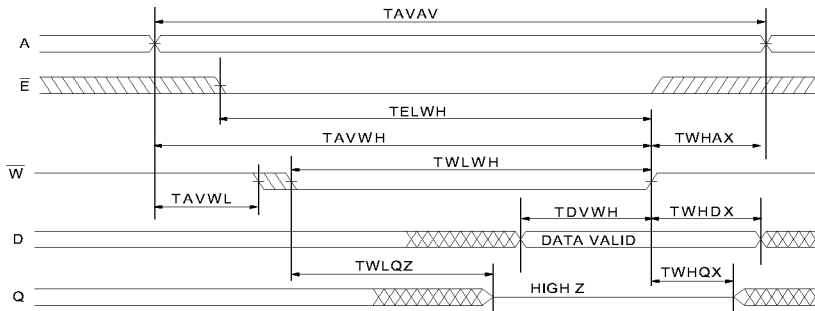


### AC Characteristics Write Cycle

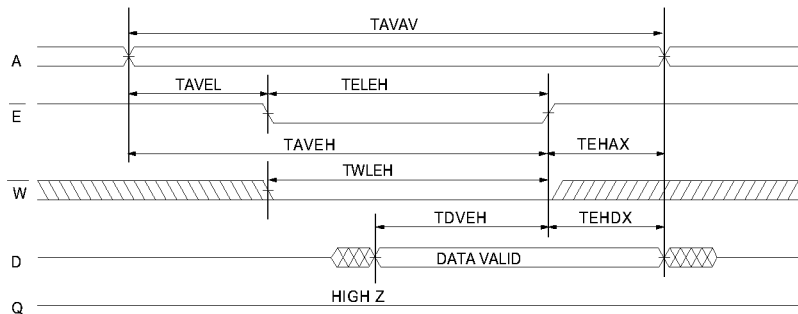
Parameter	Symbol		20ns		25ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	20		25		35		45		55		ns
Chip Enable to End of Write	TELWH	TCW	15		20		30		35		40		ns
	TELEH	TCW	15		20		30		35		40		ns
Address Setup Time	TAVWL	TAS	0	0	0	0	0	0	0	0	0	0	ns
	TAVEL	TAS	0	0	0	0	0	0	0	0	0	0	ns
Address Valid to End of Write	TAVWH	TAW	15		20		30		35		40		ns
	TAVEH	TAW	15		20		30		35		40		ns
Write Pulse Width	TWLWH	TWP	15		20		30		35		40		ns
	TWLEH	TWP	15		20		30		35		40		ns
Write Recovery Time	TWHAX	TWR	0	0	0	0	0	0	0	0	0	0	ns
	TEHAX	TWR	0	0	0	0	0	0	0	0	0	0	ns
Data Hold Time	TWHDX	TDH	0	0	0	0	0	0	0	0	0	0	ns
	TEHDX	TDH	0	0	0	0	0	0	0	0	0	0	ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	8	0	10	0	15	0	20	0	20	ns
Data to Write Time	TDVWH	TDW	12		15		20		25		25		ns
	TDVEH	TDW	12		15		20		25		25		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

### Write Cycle 1 - $\bar{W}$ Controlled



### Write Cycle 2 - $\bar{E}$ Controlled



**ED18C32512CA**  
512Kx32 Static Ram

**Data Retention Characteristics**

*Low Power (LP) Version Only*

(TA = -55 °C to +125 °C), (TA = -40 °C to +85 °C)

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	E ≥ VDD - 0.2V	--	1	8	mA
Chip Disable to Data Retention Time(1)	TCDR	VIN ≥ VDD - 0.2V	0	--	--	ns
Operation Recovery Time (1)	TR	or VIN ≤ 0.2V	TAVAV*		--	ns

Note 1: Parameter guaranteed, but not tested.

\*Read Cycle Time

**Data Retention  $\bar{E}$  Controlled**

### Ordering Information

#### Military, Standard Power

Part No.	Speed (ns)	Package No.
EDI8C32512CA20JM	20	304
EDI8C32512CA25JM	25	304
EDI8C32512CA35JM	35	304
EDI8C32512CA45JM	45	304
EDI8C32512CA55JM	55	304
EDI8C32512CA20EQ	20	405
EDI8C32512CA25EQ	25	405
EDI8C32512CA35EQ	35	405
EDI8C32512CA45EQ	45	405
EDI8C32512CA55EQ	55	405

#### Military, Low Power

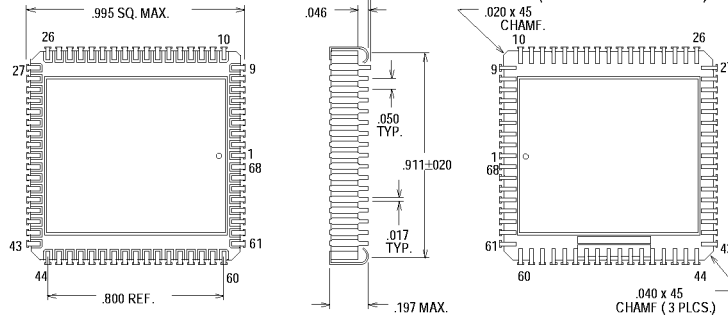
Part No.	Speed (ns)	Package No.
EDI8C32512LPA20JM	20	304
EDI8C32512LPA25JM	25	304
EDI8C32512LPA35JM	35	304
EDI8C32512LPA45JM	45	304
EDI8C32512LPA55JM	55	304
EDI8C32512LPA20EQ	20	405
EDI8C32512LPA25EQ	25	405
EDI8C32512LPA35EQ	35	405
EDI8C32512LPA45EQ	45	405
EDI8C32512LPA55EQ	55	405

For Commercial or Industrial grade product C or I replaces M in part number, e.g. EDI8C32512CA20JM becomes EDI8C32512CA20JI (Industrial temp range).

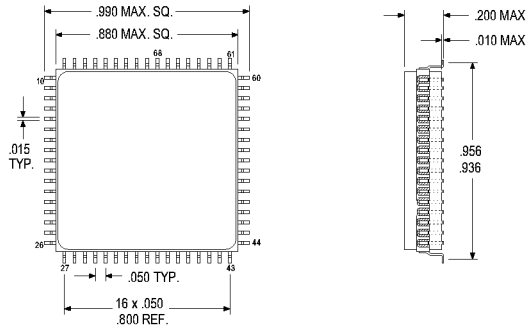
### Package Description

#### 68 Lead Ceramic JLCC

Weight = 8gm  
 Theta JC = 6 °C/W  
 Theta JA = 15 °C/W



#### 68 lead CQFP



#### Electronic Designs Incorporated

• One Research Drive • Westborough, MA 01581USA • 508-366-5151 • FAX 508-836-4850 •  
**Electronic Designs Europe Ltd.** • Shelley House, The Avenue • Lightwater, Surrey GU18 5RF  
 United Kingdom • 01276 472637 • FAX: 01276 473748  
<http://www.electronic-designs.com>

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